Back-Illuminated Double-Avalanche-Region Single-Photon Avalanche Diode

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(Invited Paper)

***Abstract*—The key features of a single-photon avalanche diode (SPAD) are its ability to detect a single photon and provide a digital signal output. The avalanche multiplication process, which generates a detectable electrical signal that can be amplified up to a high voltage without the need for additional circuits, allows SPADs to detect individual photons. Specifically, a SPAD fabricated in CMOS technology can detect near-infrared (NIR) signals, which is a crucial requirement in many applications such as light detection and ranging (LiDAR), time-of-flight (ToF) imaging, and NIR optical tomography. These applications require specific performance characteristics, for example, high photon detection probability (PDP). In this article, we propose an optimized SPAD developed based on 40 nm backside illuminated (BSI) CMOS image sensor (CIS) technology. The SPAD is designed and fabricated using a heavily doped p-type (P+) and a retrograde doped deep n-well (DNW) junction. The doping-optimized guard-ring (GR) for the expansion of the avalanche multiplication region maximizes PDP, while maintaining its original capability, premature edge breakdown (PEB) prevention at the edge of the junction. We demonstrate the effectiveness of GR optimization by comparing the electrical and optical experimental results with the conventional SPAD. The proposed double-avalanche-region (DAR) SPAD achieves a peak PDP of about 89% at the wavelength of 700 nm and a PDP of 45% at 940 nm, which are the highest values among SPADs reported so far at the excess bias voltage of 2.5 V. The dark count rate (DCR) is 27 cps/μm^2 and the full width at half-maximum (FWHM) of the timing jitter is 89 ps at the same operating condition.**

***Index Terms*—Avalanche photodiode (APD), back-illuminated single-photon avalanche diode (SPAD), CMOS image sensor (CIS) technology, detector, diode, electronic-photonic integration, geiger-mode avalanche photodiode (G-APD), high-volume manufacturing, integrated optoelectronics, integration of photonics in standard CMOS technology, light detection and ranging (LiDAR), near infrared (NIR), optical sensing, optical sensor, photodetector, photodiode, photomultiplier, RGB-D sensor, semiconductor device, sensor, silicon, wafer-scale.**

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I. Introduction

A SINGLE-PHOTON avalanche diode (SPAD) is an optoelectronic device capable of detecting a single photon and providing a digital output signal. The basic structure of a SPAD is based on a p-n junction diode, engineered to operate in Geiger mode by reverse-biasing above its breakdown voltage (V_B). The abilities to detect a single photon and to generate a digital output make SPADs a key enabling technology in a wide range of applications, spanning from time-of-flight (ToF) imaging systems to quantum applications. Due to their operating principle and versatility across various applications, SPADs have been the subject of continuous study and development. Additionally, fabricating SPADs using CMOS technology offers several advantages, such as integration with electronics, scalability, cost-effectiveness, and high-density SPAD arrays. As a result, SPAD development has advanced in various CMOS processes since the work by E. Charbon [1]. The typical way of fabricating a CMOS SPAD is using frontside illumination (FSI) processes which has the advantages of a simple fabrication process and high yield [1], [2], [3], [4], [5], [6], [7], [8], [9]. However, the most critical limitation of the FSI approach is reduced sensitivity to light because the metal layers and electronic components on the front side can block or scatter the incoming photons. To overcome this limitation, SPADs have been developed using backside illumination (BSI) processes [10], [11], [12], [13], [14], [15], [16], [17]. The BSI technology enhances the sensitivity of SPADs because there are no components blocking the incoming photons. In addition, the thickness of the remaining Si wafer after the backside thinning can be adjusted to optimize the SPAD performance for each target wavelength range. Recently, the most desirable applications based on CMOS SPADs are light detection and ranging (LiDAR) for smartphones and autonomous vehicle systems at near-infrared (NIR) wavelengths, and SPADs based on the BSI technology have deeper avalanche multiplication regions and thicker absorption regions, providing the advantage of higher

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chance of detecting carriers generated by NIR photons. One of the most important factors in evaluating the performance of a SPAD is the photon detection probability (PDP), which represents the probability that an incident photon triggers an avalanche multiplication. There are various advantages to the systems when improving PDP in SPAD-based sensors. First, in a ToF system [18], [19], [20], a high PDP can enable the detection of a weaker return signal, which may allow for the use of a lower-power laser source, leading to reduced power consumption. Also, the system can more effectively distinguish true signals from the background noise, leading to the improved signal-to-noise ratio (SNR). And higher PDP means that the detector is more likely to detect weak return signals accurately, allowing better detection of distant or low-reflectivity objects in LiDAR applications. There are several ways to improve the PDP of the SPAD fabricated in BSI technology by using specialized process options such as microlens and backside trench guide. However, these processes can increase process complexity and, consequently, result in increased fabrication cost.

In this article, in order to improve the PDP performance, we propose a double-avalanche-region (DAR) SPAD which has an expanded avalanche multiplication region with doping optimization. The DAR SPAD is fabricated in 40 nm CMOS image sensor (CIS) technology which is the most advanced technology for CMOS SPADs reported to date. The full performance of the DAR SPAD is clearly characterized and analyzed, and the electrical and optical characteristics of the conventional SPAD and the DAR SPAD are compared to prove the effectiveness of the optimization. Through the optimization, the DAR SPAD achieves an excellent PDP of 45% at the wavelength of 940 nm along with a small timing jitter of 89 ps at the full width at half maximum (FWHM).

The structure of this article is outlined as follows. Section II proposes the DAR SPAD structure and explains how the proposed SPAD is optimized. In Section III, measurement results such as the current-voltage (I-V) characteristics, dark count rate (DCR), temperature dependency, PDP, and timing jitter are presented. A comparative evaluation with other state-of-the-art SPADs is offered in Section IV. Finally, the article is concluded in Section V.

II. Device Structure and Simulation Results

In a SPAD, there are two mechanisms that can affect triggering the avalanche multiplication of the charge carrier in response to an electric field [21]. First, drift is the movement of the charge carriers caused by an electric field. When a reverse bias is applied to a SPAD through the p-n junction, it exerts a force on the charge carriers, causing them to quickly move to the avalanche multiplication region. Secondly, diffusion is the process by which charge carriers move from an area of higher concentration to an area of lower concentration. Diffusion is less related to the electric field compared to the drift, but the electric field can affect the behavior of diffusion indirectly by altering the concentration gradient of the carriers, which in turn affects the rate of diffusion [22], [23], [24]. In a SPAD, both drift and diffusion can affect PDP, and the importance of each mechanism depends on the device design and operating conditions. To improve the PDP of the SPAD in the BSI process, several techniques were introduced as mentioned in Section I, such as microlens and backside trench guide. However, implementing an additional structure requires specialized equipment and processes, which are more difficult to control and result in higher manufacturing costs. The most cost-effective and simple way is optimizing the doping concentration without any addition to expand the avalanche multiplication region and carrier collection region that can directly affect PDP as shown in Fig. 1. Even if the drawn active areas are the same as the P-Type region in Fig. 1(a), (b), it is possible to extend the avalanche multiplication over the guard-ring (GR) region by optimizing the doping concentration as illustrated in Fig. 1(b). This also results in an extension of the carrier collection region, and therefore it becomes more effective at capturing the carriers generated by incident photons, leading to an increase in PDP.

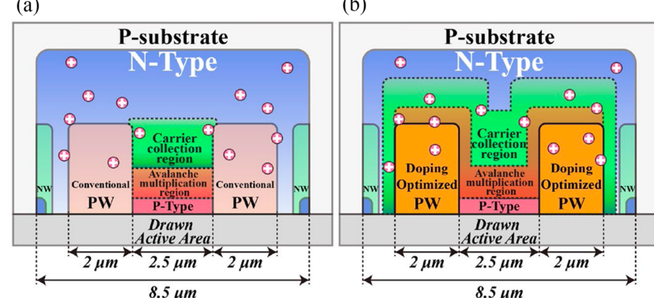

Fig. 1. Illustrated images: (a) conventional SPAD without GR doping optimization and (b) DAR SPAD with GR doping optimization.

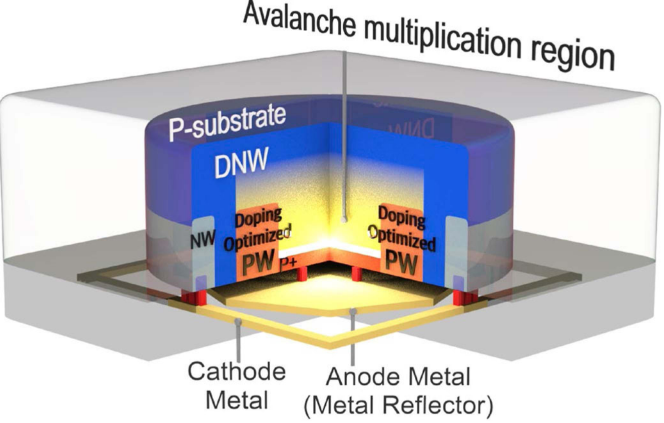

Fig. 2. Cross-section of the DAR SPAD.

In order to check and demonstrate the proposed technique, as shown in Fig. 2, the DAR SPAD is fabricated in 40 nm BSI CIS technology based on a circular shape. The SPAD is composed of a heavily doped p-type region, P+, and retrograde doped n-type region, deep n-well (DNW), that are joined together to form a p-n junction. To prevent edge breakdown and improve PDP, the doping-optimized p-well (PW) GR is placed around the p-n junction of the SPAD. The drawn active area of the SPAD consists of the p-n junction, with a diameter of 2.5 μm, and the GR has been included with a width of 2 μm. Additionally,

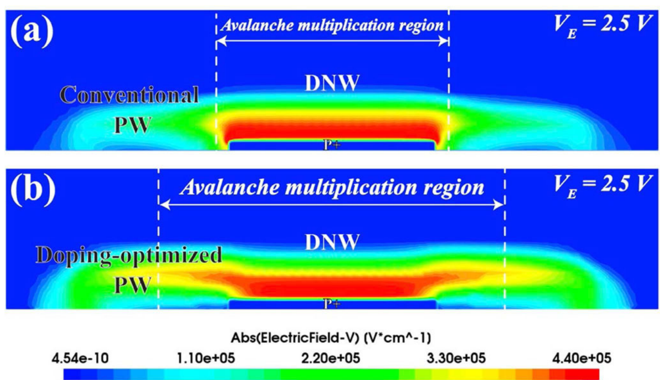

Fig. 3. E-field profile at $V_E = 2.5$ V: (a) SPAD with conventional PW GR and (b) SPAD with doping-optimized PW GR.

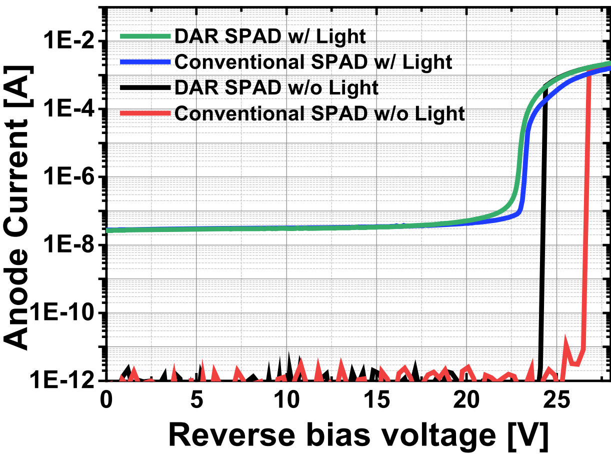

Fig. 4. Results of I-V characteristics of the two SPADs.

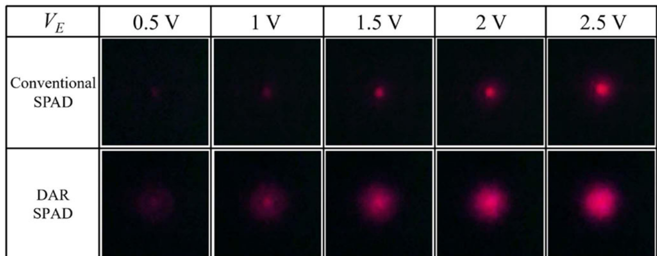

Fig. 5. Results of light-emission tests of the two SPADs at the various V_E.

to prevent breakdown and/or leakage current between GR and cathode, 0.5 μm space has been included. The device has a diameter of 8.5 μm, with a 0.5 μm cathode. The p-epi thickness is around 4 μm after the backside etching process, and it has been equipped with a metal reflector and an anti-reflection coating (ARC). The only difference between the conventional SPAD and DAR SPAD is the doping profile of their PW GRs.

The TCAD simulation was conducted to check E-field profiles of the SPADs at the excess bias voltage (V_E) of 2.5 V and the results are depicted in Fig. 3(a) and (b), showing their avalanche multiplication regions, respectively. The conventional SPAD has a lower doping concentration, which effectively prevents premature edge breakdown (PEB) at the edge of the junction but limits its ability to collect carriers generated by incident photons as shown in Fig. 3(a). On the other hand, the DAR SPAD has a higher doping concentration in the GR, which extends both the avalanche multiplication region and carrier collection region which allows for better carrier collection, resulting in a higher PDP while still preventing the PEB as shown in Fig. 3(b). In Section III, the characteristics of the two SPADs are clearly evaluated through electrical and optical experiments so that it demonstrates the effectiveness of the GR optimization.

III. Experimental Results

I-V characteristics can be used to observe the operation of a device that functions as a SPAD. The key operating method of a SPAD is the repetition of avalanche breakdown, which occurs when a high electric field is applied across the device, causing carriers to gain energy and collide with other atoms in the silicon through impact ionization. These newly released free carriers, in turn, collide with other atoms even more free carriers, and so on, leading to an avalanche effect that can cause the device to breakdown. The resulting avalanche breakdown can be observed through the I-V graph, as shown in Fig. 4. The performance of the two proposed SPADs is evaluated under both dark and ambient light conditions at room temperature. Specifically, the conventional SPAD with low GR doping concentration exhibits a V_B of 23.6 V, while the DAR SPAD with high GR doping concentration shows a slightly lower V_B of 23.3 V.

The active area of a SPAD refers to the region of the p-n junction that is sensitive to incident photons and capable of generating an avalanche breakdown when a photon is detected. To calculate the PDP of a SPAD by using the formula depicted (1), the SPAD active area is a critical parameter that needs to be determined.

$$\text{PDP}\ [\%] = \frac{\#\ of\ counts - DCR}{\left\{P_{opt}/\frac{hc}{\lambda}\right\} \times \frac{SPAD\ active\ area}{ref.\ PD\ area}} \times 100 \quad (1)$$

Typically, the *SPAD active area* is defined by the layout of the device, and the drawn active area illustrated in Fig. 1 is used for PDP calculations. However, the optimization of the doping concentration in the GR can lead to an extension of the avalanche multiplication region beyond the drawn p-n junction. When this happens, the PDP calculation based on the drawn active area may not be accurate. To define the effective active area that can be considered as the multiplication region, two measurements were conducted.

The light emission test (LET) is one of the experiments that can define the effective active area of a SPAD as the avalanche multiplication can lead to the emission of photons [25], [26], [27]. These photons can be detected using a microscope and image sensor and can help estimate the effective active area of a SPAD. The results of the LETs, as shown in Fig. 5, indicate the emission of light due to avalanche multiplication at various voltage levels, from $V_E = 0.5$ V to $V_E = 2.5$ V in 0.5 V steps. Basically, the two SPADs do not suffer from PEB and the results provide insight into the effective active areas of the SPADs. As

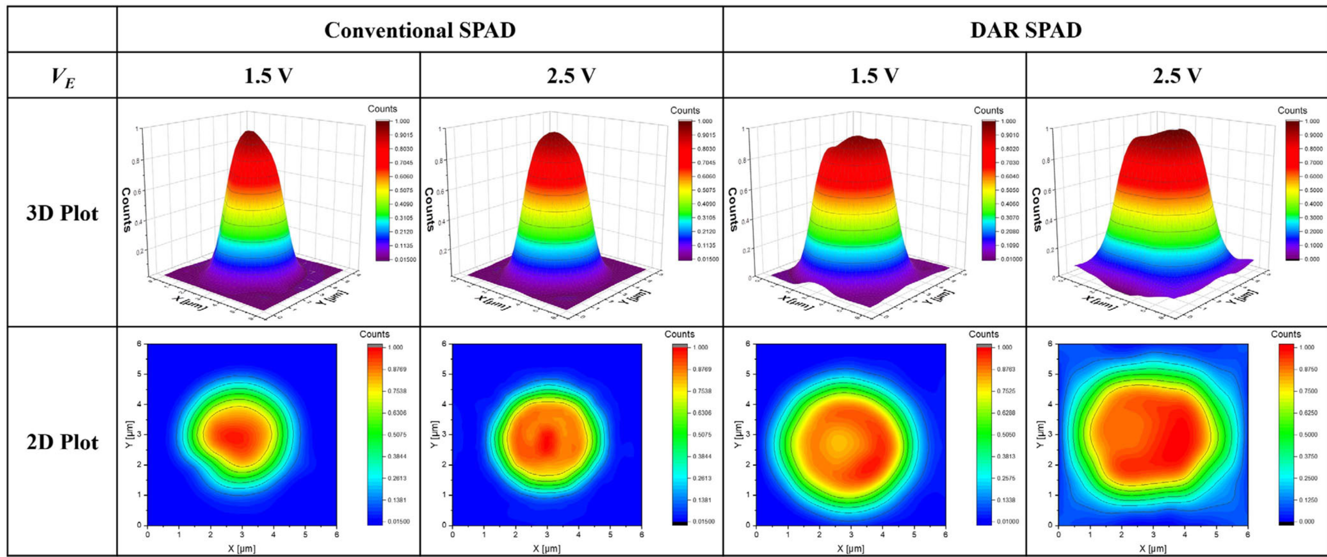

Fig. 6. Results of laser-scanning microscopy at the various excess bias voltages.

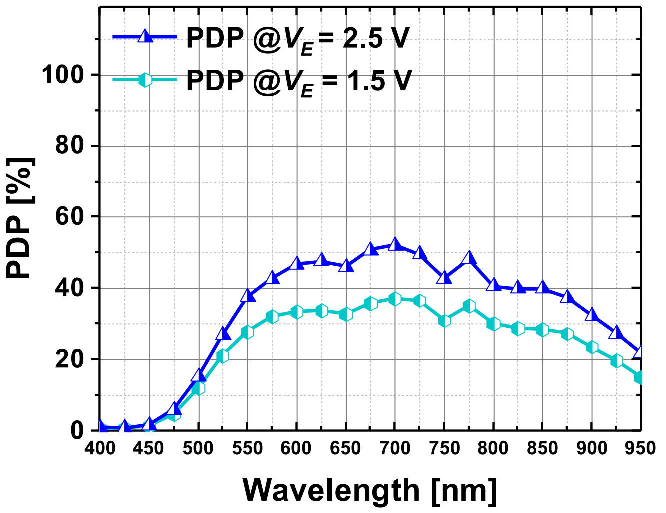

Fig. 7. PDP results of conventional SPAD.

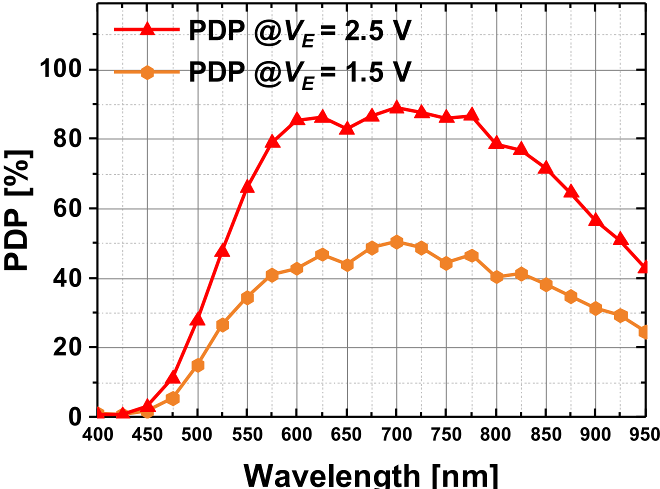

Fig. 8. PDP results of DAR SPAD.

the applied V_E increases to both conventional and DAR SPADs, the electric field becomes wider and stronger, which can be demonstrated by observing the expansion of the multiplication region through changes in both light intensity and area. Although the two SPADs have the same drawn active area, they exhibit different levels of expansion in response to increases in V_E. While all experimental conditions were the same, there was no significant difference in light intensity when comparing the LET results of the conventional SPAD and the DAR SPAD. However, it was observed that the lighting area, which presents the avalanche multiplication region, was significantly larger in the DAR SPAD. To investigate the accurate effective active areas of the two SPADs further, an experimental study using laser scanning microscopy (LSM) is conducted. The LSM experiment is used to detect the exact avalanche multiplication regions of the SPADs by measuring the number of photon pulses from the SPAD when a laser beam is scanned across the SPAD and reconstructing an image from the collected data. Specifically, a 637 nm continuous laser was used for the light source, and an oscilloscope was used as a detector to measure the number of photon pulses from the SPADs operating with a 200 kΩ external passive quenching resistor. The two fabricated SPADs were scanned at $V_E = 1.5$ V and $V_E = 2.5$ V. The data were reconstructed into 2D and 3D images, which are shown in Fig. 6. Through these results, it is possible to determine an exact dimension of the effective active area for each SPAD where the avalanche multiplication actually occurs. The drawn active area is 2.5 μm in diameter, but in the case of the conventional SPAD, there is a slight contribution from the GR side, around 2.6 μm in diameter at $V_E = 1.5$ V, and 2.9 μm in diameter at $V_E = 2.5$ V based on the FWHM count of the LSM result. On the other hand, in the case of the DAR SPAD, it was confirmed that the effective active area is 3.68 μm in diameter at $V_E = 1.5$ V, and 4.44 μm in diameter at $V_E = 2.5$ V based on FWHM count of the

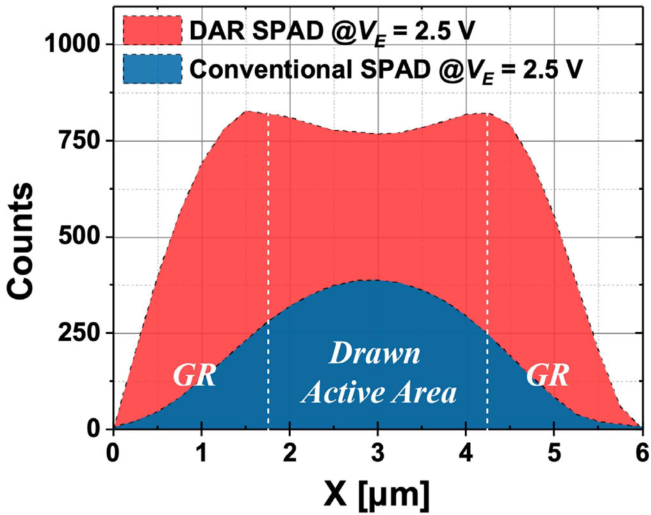

Fig. 9. Z-axis 2D cross-section of the LSM data.

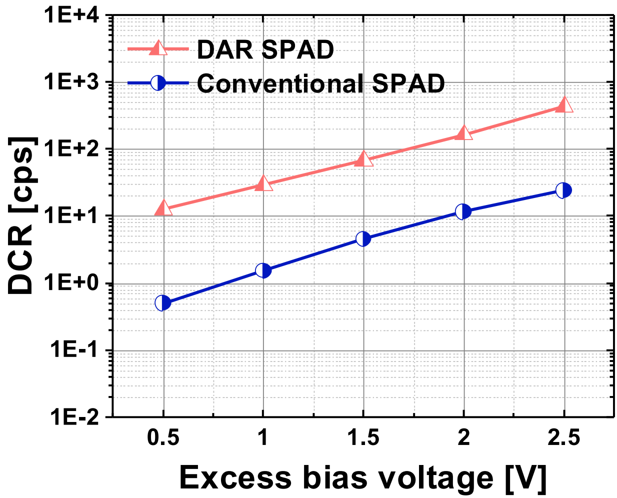

Fig. 10. DCR results of both conventional and DAR SPADs at the various V_E.

LSM result. The results clearly demonstrate that the proposed GR optimization expands the avalanche multiplication region. The LSM experimental results also confirm the LET results, as the V_E increases the DAR SPAD exhibits a wider expansion region than the conventional SPAD. Based on the experimental results obtained from both the LET and LSM studies, the actual dimensions of the effective active area were used as '*SPAD active area*' in (1) in calculating the PDP.

The PDP is determined experimentally by measuring the ratio of the number of electrical output pulses generated by the SPAD in response to the number of incident photons. The number of electrical output pulses generated by the SPAD can be measured by a high-performance oscilloscope and the number of incident photons can be calculated by the optical power incident to the SPAD using an integrating sphere and a ref. PD. PDP measurements were conducted in the range of wavelength from 400 nm to 950 nm, and the results are depicted in Figs. 7 and 8. Both conventional and DAR SPADs show low PDPs in the range of wavelength under 450 nm because the photon-generated electrons in the P-substrate cannot overcome the barrier of the other p-n junction between the P-substrate and DNW. As a result, carriers by incident photons with wavelengths between 400 nm and 450 nm at the surface of the SPAD rarely trigger avalanche multiplication. The main difference between conventional and DAR SPADs is their PDP performance beyond the wavelength of 450 nm. The conventional SPAD has a peak PDP of 52% at a wavelength of 700 nm and a PDP of 23% at a wavelength of 940 nm when $V_E = 2.5$ V. While conventional SPAD also has good PDP performance, the proposed DAR SPAD, thanks to the wider multiplication region and carrier collection region achieved through optimized doping concentration at the GR, has achieved approximately twice as high in PDP. The DAR SPAD achieves a peak PDP of 89% at a wavelength of 700 nm and a PDP of 45% at a wavelength of 940 nm when $V_E = 2.5$ V. The reason can be explained through the Z-axis 2D cross-section of the LSM data in Fig. 9. The incident optical power to both SPADs is the same but the result shows totally different shapes and counts. The number of photon counts of the DAR SPAD is more than double that of the conventional SPAD in the entire avalanche multiplication region. Especially, the GR region of the DAR SPAD shows much higher counts thanks to the larger avalanche multiplication and carrier collection regions extended vertically and horizontally.

DCR was also characterized firstly at room temperature. DCR refers to the number of counts generated by the SPAD in the absence of any incident photon. The dark count can be triggered by several types of carriers such as thermally generated carriers, trapped carriers, and surface state of both P-substrate between the dielectric side and backside etching/thinning side from the BSI process. The results for both conventional and DAR SPADs are shown below 500 cps DCR at the $V_E = 2.5$ V as depicted in Fig. 10. The DCR is proportional to the multiplication region and carrier collection region which respectively contribute to the movement of carriers. The higher DCR of the DAR SPAD compared to the conventional SPAD can be attributed to its wider effective active area and carrier collection region. However, the SPAD exhibits sufficiently low DCR. Specifically, the DCR of DAR SPAD normalized by effective active area is about 27 cps/μm^2. The main factor that can trigger dark count in SPADs fabricated using the BSI process is the presence of dangling bonds that remain after the backside thinning/etching process. However, both SPADs are isolated from the backside etched/thinned surface of the P-substrate by DNW, so the main contributors to increasing DCR are likely to be thermally generated carriers and trapped carriers. The sources of dark counts in the proposed SPAD can be estimated by measuring them at various temperature conditions.

The DCR measurements were conducted at various temperatures in the range of $-20 \sim 80$ °C in 20 °C increments with a temperature chamber. The results for both SPADs are shown in Fig. 11 as a function of temperature at $V_E = 2.5$ V. Through the temperature-dependent DCR measurement, several factors can be defined such as DCR variation with temperature, temperature coefficient, and activation energy (E_a). The DAR SPAD exhibits a DCR of about 1.5 kcps/μm^2, an acceptable rate even when the

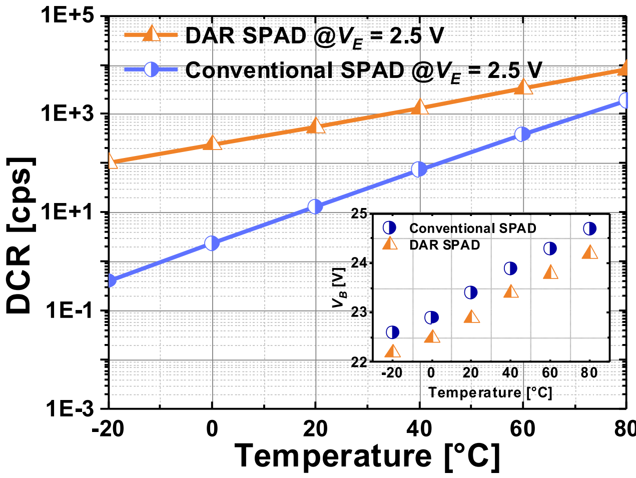

Fig. 11. Temperature-dependent DCR results of both conventional and DAR SPADs at $V_E = 2.5$ V and the temperature-dependent V_B in the inset.

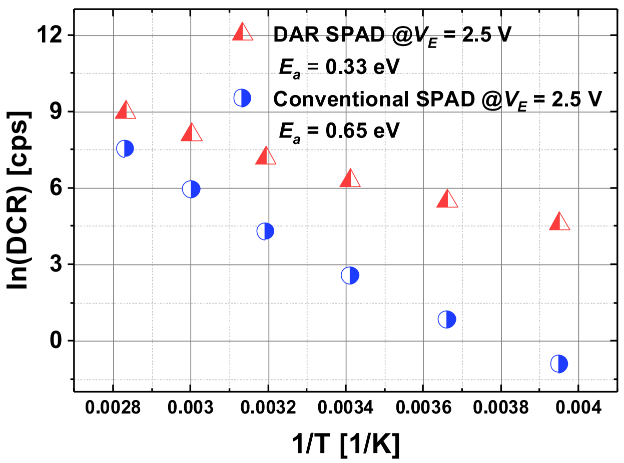

Fig. 12. Arrhenius plot of both conventional and DAR SPADs at $V_E = 2.5$ V.

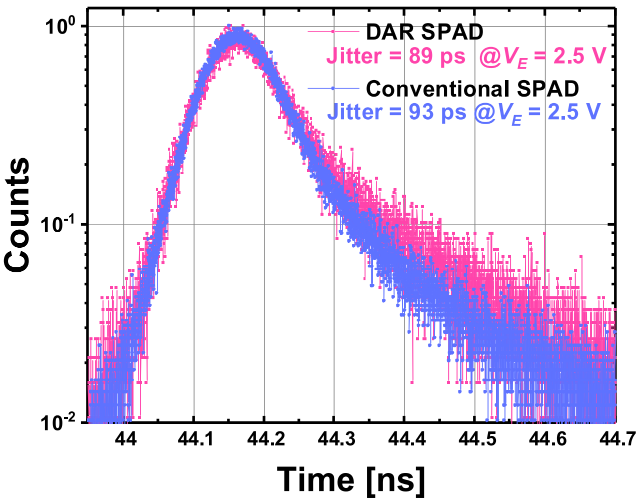

Fig. 13. Timing jitter results of both conventional and DAR SPADs at $V_E = 2.5$ V.

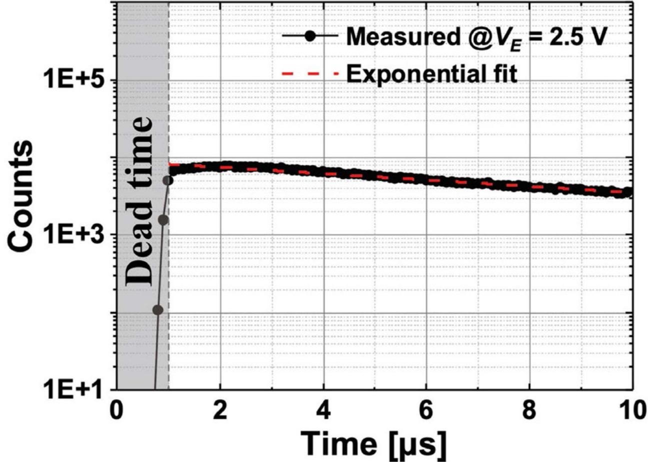

Fig. 14. Inter-avalanche time histogram of the DAR SPAD at $V_E = 2.5$ V along with a fitted exponential curve.

temperature reaches 80 °C. The conventional SPAD exhibits a DCR of about 0.4 kcps/μm^2 which is lower than DAR SPAD due to its narrower effective active area and carrier collection region. The temperature coefficient is shown to be 15 mV/K as depicted in the inset of Fig. 11. This result confirms that DAR SPADs exhibit low changes in V_B and DCR with temperature. Thanks to these advantages, the proposed SPAD can be employed in various applications that require temperature-hardened devices. The activation energy is also extracted from the Arrhenius plot, depicted in Fig. 12. The E_a of the conventional SPAD has been calculated as 0.65 eV and the E_a of the DAR SPAD as 0.33 eV at $V_E = 2.5$ V. The main contributor of the DCR can be the ion implantation of phosphorus, and it is estimated that the dominant noise mechanism of the DAR SPAD is trap-assisted tunneling while that of the conventional one is trap-assisted thermal generation.

Fig. 13 shows the results of timing jitter measurements of both SPADs conducted when $V_E = 2.5$ V at room temperature. Both the conventional and DAR SPADs were measured under the same conditions using a 940 nm picosecond pulsed laser as a light source and employing the time-correlated single-photon counting (TCSPC) technique with a high-speed oscilloscope. The period of the pulsed laser was carefully adjusted using a neutral density filter to prevent distortion of the jitter measurement. The timing jitter of the conventional SPAD is 93 ps at the FWHM, while that of the DAR SPAD is 89 ps at the FWHM. Considering the timing jitter of the SPADs, the spatial uncertainty in distance measurements can be estimated. The 89 ps timing jitter of the DAR SPAD results in a distance measurement uncertainty of approximately 13.3 mm and the spatial uncertainty of conventional SPAD is 13.9 mm. Both SPADs have similar FWHM values but the diffusion tail of the DAR SPAD is a little bit longer because its carrier collection region is wider than the conventional SPAD.

To evaluate the inter-avalanche time histogram of the DAR SPAD at $V_E = 2.5$ V, we used a 200 kΩ external passive quenching resistor. The result is depicted in Fig. 14, and the dead time is about 1 μs. The result indicates afterpulsing probability at this dead time is negligible.

TABLE I
SUMMARY AND COMPARISON OF THE STATE-OF-THE-ART BACK-ILLUMINATED SPADS

Parameter	Unit	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[17]	**This work**
Technology	-	130 nm CMOS	130 nm CMOS	65 nm CIS	65 nm CIS	45 nm CIS	140 nm SOI CMOS	90 nm CIS[α]	90 nm CIS[α]	**40 nm CIS**
Junction	-	P+/N-well	NLDD/PW	PW/DNW	PW/DNW	P+/DNW	P+/N-well	n.a.	n.a.	**P+/DNW**
Guard ring	-	PW	NW	Virtual GR	Virtual GR	PW	PW	n.a.	n.a.	**PW**
Shape	-	Round	Round	Round	Fermat	Round	Round	n.a.	n.a.	**Round**
Active area	μm^2	28.3	28	27.6	n.a.	122.7	113	n.a.	n.a.	**15.47**
V_B	V	12.3	16.5	12	n.a.	28.5	11.3	30	22	**23.3**
V_E	V	4	1.5	3	4.4	2.5	3	2.5	3	**2.5**
DCR	cps/μm^2	265.3	1250	391.4	2463.1	55.4	396.1	0.044	19[β]	**27**
Peak PDP (Wavelength)	%	11 (@725 nm)	13 (@700 nm)	27.5 (@640 nm)	29 (@660 nm)	31.8 (@600 nm)	26 (@500 nm)	69.4[γ] (@510 nm)	50.5[δ] (@800 nm)	**89 (@700 nm)**
PDP @905 nm	%	n.a.	n.a.	9	8	9	8	28.7[γ]	31.9[δ]	**58**
PDP @940 nm	%	n.a.	n.a.	7.5	5.5	7	6.5	24.4[γ]	20.5[δ]	**45**
Timing jitter (Wavelength)	ps	n.a.	505 (@750 nm)	205 (@773 nm)	95 (@700 nm)	107.7 (@637 nm)	119 (@637 nm)	100 (@940 nm)	137 (@940 nm)	**89 (@940 nm)**

[α]with microlens, [β]cps/pix, [γ]PDE with microlens and pyramid surface, [δ]PDE with microlens and light trapping

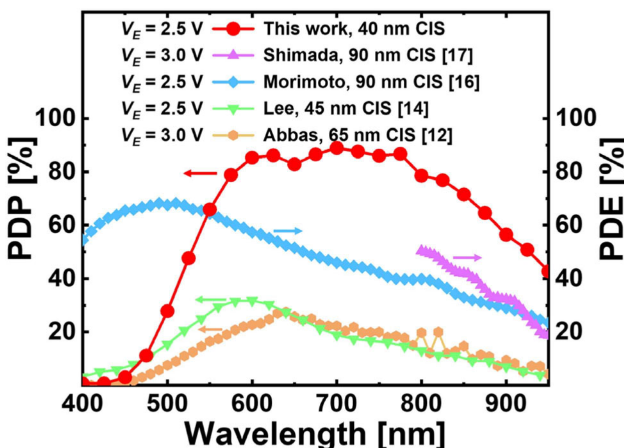

Fig. 15. PDP comparison of the state-of-the-art SPADs.

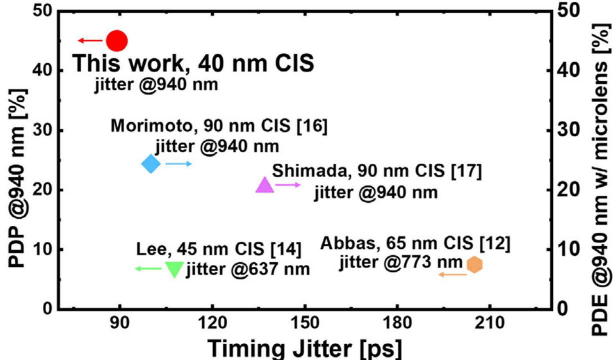

Fig. 16. Performance comparison of SPADs: PDP at 940 nm vs timing jitter.

IV. Comparison and Discussion

Fig. 15 shows the achieved PDP with the proposed SPAD in comparison to the state-of-the-art SPADs. As shown in this graph, [16] shows high photon detection efficiency (PDE) with the charge-focusing technique and light trapping engineering. Also, the PDE of [17] is as good as [16] at the NIR wavelength range due to the effect of the pyramid surface for diffraction at the backside surface of the SPAD along with the use of 7 μm thick epi. Since a microlens is built on each of the SPADs, the PDE can be considered as PDP by assuming that their fill factors are 100% with the microlens. Thanks to the wide carrier collection region, high E-field, metal reflector, and ARC as well as the optimized backside process based on the advanced CIS technology, the proposed DAR SPAD shows higher PDP values in the NIR range, where LiDAR sensors and 3D imagers operate. In case we compare the efficiency the other way around, i.e., in terms of PDE rather than PDP, with assuming that a microlens will concentrate all the incident photons into the effective active area, the contribution of the carrier collection region should be excluded. Therefore it is expected that the maximum achievable PDE is 92% of the PDP, as the contribution of the carrier collection region outside the active area is about 8% which is estimated with the LSM result shown in Fig. 6.

In addition, thanks to the wide and high E-field at the junction and the use of an isolated structure, it achieves superior timing jitter, which is the best performance of any BSI SPADs reported so far as shown in Fig. 16. The overall performance of the proposed SPAD is summarized in Table I, which also shows the comparisons with the state-of-the-art SPADs.

V. Conclusion

We propose and demonstrate a DAR SPAD with GR-region doping optimization in 40 nm BSI CIS technology. Through the LET and LSM, the effective active area is clearly demonstrated, and the expansion of the avalanche multiplication region over the GR region is proved. The device is fully characterized, including PDP, temperature-dependent noise characteristics, and timing jitter. Thanks to the wide effective active area and carrier collection region, high E-field at the planar junction, optimized backside process, metal reflector, and ARC, the DAR SPAD achieves a DCR of 27 cps/μm^2, peak PDP of 89% at 700 nm, PDP of 45% at 940 nm, and timing jitter at 940 nm of 89 ps all at $V_E = 2.5$ V. The SPAD achieves, to the best of our knowledge, the highest PDP and the lowest timing jitter among reported BSI SPADs so far. We expect that the proposed SPAD can play a key role in various applications.

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